AVIGNYA GAUTAM

Electronics, Communication & Information Engineer · Embedded Systems & AI Researcher · IEEE Leader

Kathmandu, Nepal | +977 9847690221 | gautamavignya@gmail.com | linkedin.com/in/avignya-gautam | github.com/entalecia

PROFESSIONAL SUMMARY

High-achieving Electronics, Communication & Information Engineering student (**CGPA: 3.77/4.00, Top 5% of Cohort, 1st Semester College Topper**) with hands-on expertise across **embedded systems, digital hardware architecture (FPGA/Verilog), machine learning (CNNs, XGBoost), and full-stack software development**. **1st Place National Winner of the 2026 IEEE CASS Student Design Competition**, Principal Investigator of a **US $1,420 IEEE EPICS/IMS Grant**, and **2026 IEEE IMS Global Student Ambassador**. Published author with a proven track record of taking complex hardware–software systems from circuit design and mathematical modeling to real-world deployment.

EDUCATION

Bachelor of Engineering in Electronics, Communication & Information Engineering (BEI) **2024 – Present (7th Sem)**

Thapathali Campus, Institute of Engineering (IOE), Tribhuvan University | Kathmandu, Nepal

- **Academic Distinction:** Cumulative GPA: **3.77 / 4.00** (Peak Semester GPA: **3.80 / 4.00**; **Top 5% of Class**). Awarded **1st Semester College Topper** (Academic Excellence Award).
- **Relevant Coursework:** Computer Organization & Architecture, Digital Logic Design, Microprocessors, Electronic Devices & Circuits, Embedded Systems, Signals & Systems, Control Systems, Advanced Electronics, Analysis of Algorithms, Probability and Statistics.
- **Academic Governance:** Elected Class Representative (BEI 2080 Cohort, 45 students); primary liaison between faculty and students for curriculum and laboratory coordination.

Higher Secondary Education (+2 Science, Physics & Mathematics) **2021 – 2023**

St. Xavier's College, Maitighar | Kathmandu, Nepal

- **Academic Standing:** Cumulative GPA: **3.77 / 4.00** (Peak GPA: **3.81 / 4.00**). Event Coordinator for SX3C Computer Club; Active Member of SEDS-SXC (Space Exploration & Development Society); Daily Math/Science Tutor at PiE Initiative (6–8 AM).

TECHNICAL SKILLS

Programming & HDL	Python, C, C++, Verilog HDL, JavaScript, SQL, MATLAB, Bash / Shell Scripting, LaTeX
AI, Machine Learning & DSP	Deep Learning, 1D Convolutional Neural Networks (CNNs), Siamese Neural Networks, Gradient-Boosted Decision Trees (XGBoost), Supervised Learning, Digital Signal Processing (Butterworth & Sallen–Key Filtering, Hilbert Transform), Data Cleaning & Statistical Analysis
Hardware, Embedded & IoT	ESP32 / ESP32-S3, FreeRTOS, Hardware Timer Interrupts (ISR), Field-Programmable Gate Arrays (FPGA), Register-Transfer Level (RTL) Design, Printed Circuit Board (PCB) Layout (EasyEDA, Proteus), Analog Front-End (AFE) Conditioning, I2C / SPI / UART / GSM Telemetry, PLC, 3D CAD
Software, Web & Tools	Linux, Git / GitHub, Flask, RESTful Web APIs, Full-Stack Web Portals, Automated Data Pipelines, VS Code

EXPERIENCE & LEADERSHIP

Founder & Chair | 2026 Global Student Ambassador **2025 – Present**

IEEE Thapathali Student Branch (STB60233766) | Kathmandu, Nepal

- **Institutional Founding & Scale:** Founded the first-ever IEEE Student Branch at Thapathali Campus; directed **15+ national technical competitions, hackathons, and hardware bootcamps for 1,000+ attendees** (including IEEEXtreme 19.0, IEEE CASS SDC, and ESP32-S3 PCB design workshops).
- **Grant & Project Management:** Secured a **US $1,420 EPICS in IEEE & IEEE IMS Project Grant** as Principal Student Investigator, leading cross-functional engineering teams, hardware procurement, NGO stakeholder alignment, and financial compliance.
- **Global Representation:** Selected as a **2026 IEEE IMS Global Student Ambassador** (one of ∼25 worldwide), **IEEE Day 2025 National Representative for Nepal**, and **Volunteer Judge for the IEEE Solid-State Circuits Society (SSCS) Global Arduino Contest**.

Research Assistant (Under Prof. Dr. Dhruba Kumar Gautam) **2023 – Present**

Nepalese Academy of Management (NAM) | Kathmandu, Nepal

- **Data Engineering & Empirical Analytics:** Architected large-scale quantitative and qualitative survey data acquisition pipelines; engineered automated data cleaning, validation, and statistical analysis workflows for academic research studies.
- **Full-Stack Web Infrastructure:** Designed, deployed, and maintained the Academy's official web platform and digital registration systems, improving platform reliability, user accessibility, and publication indexing.
- **International Conference Operations:** Coordinated the technical secretariat, peer-review submission workflows, and digital proceedings for international research conferences hosting **500+ scholars, keynote speakers, and institutional delegates**.

Senior Research Advocate **2024 – 2025**

TENSOR (Technical & AI Research Group, IOE Thapathali) | Kathmandu, Nepal

- Conducted applied research on modern deep learning architectures and computer vision; designed and delivered hands-on AI/ML and programming workshops to **200+ students** across high schools in the Kathmandu Valley.

TECHNICAL PROJECTS

Autonomous Solar-Powered River Water Monitoring Buoy | *ESP32-S3, 4G LTE IoT, MPPT Solar* **2026 – Present**

- Awarded **US $1,420 by EPICS in IEEE & IEEE IMS** as Project Lead to build a real-time water quality telemetry buoy in partnership with non-profit Clean Up Nepal for deployment in Kathmandu's Bagmati River.
- Designed an ultra-low-power architecture around an **ESP32-S3** using deep-sleep duty cycling (30-minute wake intervals), **20W MPPT solar charging with a 10Ah LiFePO4 battery**, and buck/boost DC–DC regulation for **7-day zero-sunlight autonomy**.
- Integrated a 5-channel industrial sensor array (pH, Dissolved Oxygen, Turbidity, TDS, Temperature) with edge noise filtering, **4G LTE GSM cloud telemetry**, and an automated **IP67 high-torque servo wiper** (6-hour cycle) to prevent sensor biofouling.

16-Bit Harvard-Architecture RISC Processor | *Verilog HDL, Digital Architecture, | [GitHub]* **2026**

- Designed and implemented a custom 16-bit RISC central processing unit from scratch in **Verilog HDL** featuring a decoupled **Harvard instruction and data memory datapath** for concurrent instruction fetch and data access.
- Built and verified modular RTL components including a 16-bit Arithmetic Logic Unit (ALU), dual-port register file, instruction decoder, sign-extension unit, and branch/jump Program Counter (PC) control unit via behavioral testbenches.

Predictive Vascular Age & Stiffness Estimation System | *ESP32, FreeRTOS, Analog PCB, 1D-CNN* **2026**

- Engineered a **4-stage low-noise Analog Front-End (AFE)** using **LMV324** operational amplifiers to capture microvolt-level piezoelectric heart sounds (PCG) simultaneously with optical photoplethysmography (**MAX30102** PPG).
- Programmed deterministic multi-rate data acquisition on an **ESP32** using **FreeRTOS task isolation and hardware timer interrupts (ISR)**, achieving < 5 **ms inter-channel synchronization latency** alongside a Python web diagnostic dashboard.
- Developed a signal processing and machine learning pipeline applying **4th-order Butterworth filtering** and **Hilbert transform envelope extraction** to drive a dual-pathway **XGBoost** and **1D-CNN (Net1D)** model within **ISO 81060-2** clinical accuracy bounds.

Six Sense Haptic Braille Mechatronic Device | *Custom PCB, ESP32, Flask Web Server, 3D Mechatronics* **2025**

- Won **1st Place Nationally (IEEE Nepal Section)** and advanced to **IEEE Region 10 Phase 2** in the **2026 IEEE Circuits and Systems Society (CASS) Student Design Competition**.
- Built a rechargeable assistive reading device for visually impaired users featuring a custom PCB, 3D-printed housing, and a **Flask web server** communicating with an **ESP32** to drive a closed-loop array of three servo motors into tactile Braille patterns.

Neural Network from Scratch & Siamese Verification Pipeline | *Python, C, Linear Algebra, Deep Learning* **2025**

- Built a multi-layer neural network from first principles without high-level ML frameworks, implementing forward matrix propagation, backpropagation, and gradient descent optimization from scratch; directly underpinned a peer-reviewed journal publication.

RESEARCH PUBLICATIONS

- **[Peer-Reviewed Journal]** A. Adhikari, I. Sharma, and **A. Gautam**, "Signature Verification using Siamese Neural Network," *International Journal on Engineering Technology (InJET)*, vol. 3, no. 1, pp. 188–194, Dec. 2025.